FOUR-WATT 20-GHz PARTIAL MONOLITHIC AMPLIFIER

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ABSTRACT

A 4-watt power amplifier with 28-percent power-added efficiency at 20 GHz has been demonstrated using 0.25-μm heterostructure FET (HFET) device technology. The 4-watt, two-stage amplifier features a mostly monolithic approach with a portion of the input and output matching networks on alumina. The output matching network employs reactive matching elements on GaAs, followed by a Chebyshev coupled-line transformer/combiner on alumina to achieve a low-impedance match with minimal loss. This paper presents discrete 0.25-μm HFET device results at 18 GHz and 20 GHz, as well as amplifier design and performance over a >3 GHz band.

INTRODUCTION

Figure 1 shows the measured output power as a function of frequency for a number of Texas Instruments monolithic circuits. Power results from FET type amplifiers are indicated by triangles, HBT power results are indicated by diamonds, and pseudomorphic HEMT (pHEMT) amplifier results are indicated with circles. Included on this chart are the results reported in this paper, 4-watts at 20 GHz, with the notation that they represent a partial monolithic circuit. The output power above 10 GHz appears to follow a 6 dB/octave roll-off.

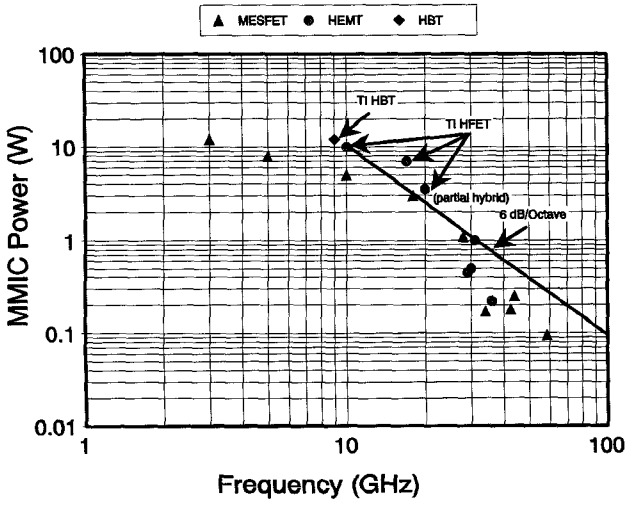

Figure 1. Power Performance of MMIC Amplifier

DEVICE TECHNOLOGY

The material structure used in the 4-watt amplifier is shown in Figure 2.[1] It includes a thin GaAs layer low-doped (mid 10^{17} cm^{-3}) and sandwiched between a superlattice buffer layer on the bottom and a low-doped (mid to high 10^{16} cm^{-3}) AlGaAs. A n+ GaAs cap layer completes the structure. The device structure includes a 1.5-μm-wide "recess" etched into the GaAs n+ layer and into the AlGaAs low-doped layer and a conventional gate recess. Gate length is 0.25 μm. Typical

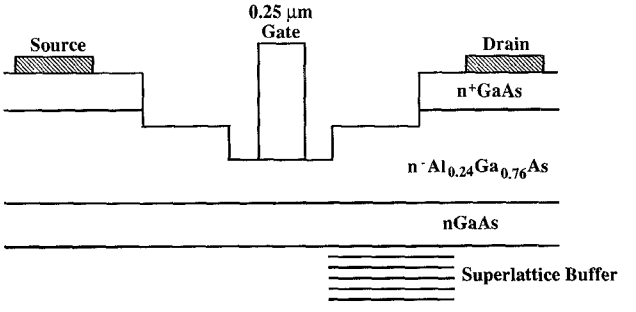

Figure 2. AlGaAs Heterostructure FET

I-V characteristics are shown in Figure 3. "Flat" characteristics (low output conductance), constant transconductance with gate voltage, and high breakdown voltage can be observed.

DEVICE RF RESULTS

Table 1 shows the average measured performance for a number of 0.25-μm HFET devices at 18 and 20 GHz. RF performance for discrete 600-μm devices was measured in a 3.5-mm fixture with prematched networks. Tuning chips were placed on the matching elements to optimize the RF performance at each frequency.

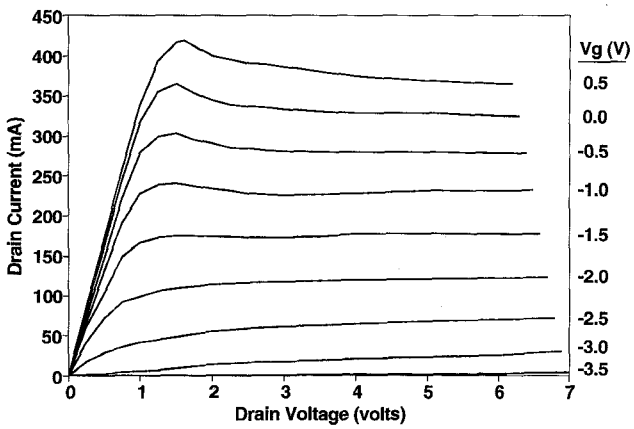

Figure 3. AlGaAs/GaAs HFET I-V Characteristics

TABLE 1. 18-AND-20 GHz 0.25 x 600-μm HFET PERFORMANCE

Frequency	Power (dBm)	Gain (dB)	PAE (%)
18 GHz	24.4	6.9	50
20 GHz	24.1	6.1	45

AMPLIFIER DESIGN

A photograph of the 4-watt, 20-GHz mostly monolithic amplifier is shown in Figure 4. The GaAs portion of the amplifier is 148 × 268 × 4 mils^3. The input network uses both GaAs and 5-mil alumina matching networks. The alumina network provides a three-way signal splitter with three sections of quarter-wave transformers. The partial input matching network on alumina was selected for two reasons: (1) it minimizes the size of the GaAs MMIC, and (2) the insertion loss of quarter-wave transmission lines is lower on highly polished alumina than it is on GaAs. The GaAs portion of the input network includes those elements that are more monolithic in nature, such as capacitors and resistors. The transition point between the GaAs MMIC and the alumina network occurs at a point where small variations in the bond wire inductance can be tolerated. The GaAs portion of the input circuitry includes a shunt stability network, an input blocking capacitor, and shunt and series transmission lines close to the device and critical to the input match. Gate bias for the 3 × 800-μm input FETs is applied through bond pads on either side of the GaAs chip.

The interstage network uses shunt and series transmission lines, as well as a shunt capacitor to match the 2.4-mm input to the 7.2-mm output stage. Drain bias for the first stage as well as gate bias for the second stage, are applied at bond pads along the GaAs chip edge.

The output network uses reactive matching elements on the GaAs circuit to tune out the device capacitance, while the real part of the load line is provided by the Chebyshev coupled-line transformer.[2] The Chebyshev coupled-line transformer provides a 14 GHz-to-40 GHz, 50Ω-to-4Ω real transformation. This network was originally designed using SCOMPACT multi-coupled line analysis, but minor deviations from that design were necessary for optimum operation. Again, the output combiner is fabricated on highly polished 10-mil alumina for two reasons: (1) it minimizes the size of the GaAs MMIC, and (2) the insertion loss of the output combiner on alumina is lower than it would be on GaAs.

AMPLIFIER RESULTS

Figure 5 is a photograph of the packaged 4-watt amplifier. RF connections are made to the amplifier with coaxial K-connectors. Four DC feedthrough pins provide drain and gate bias to the two-stage amplifier. The 4-watt amplifier was processed with both 0.25-μm delta-gate and 0.25-μm T-gate HFET devices. Figure 6 shows the power and efficiency performance for the packaged amplifier processed with 0.25-μm delta-gates. The amplifier maintains an output power

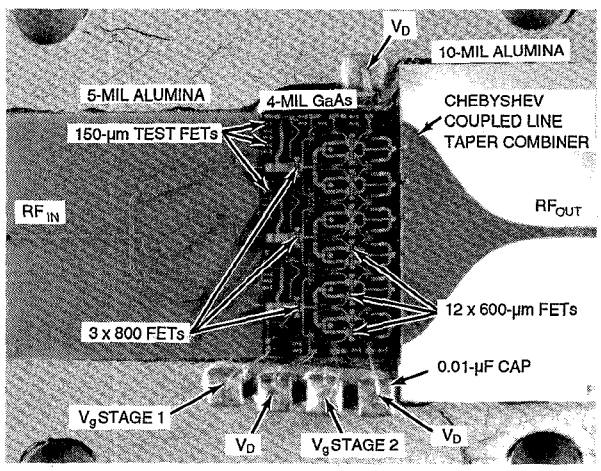

Figure 4. Two-Stage 4-Watt Amplifier

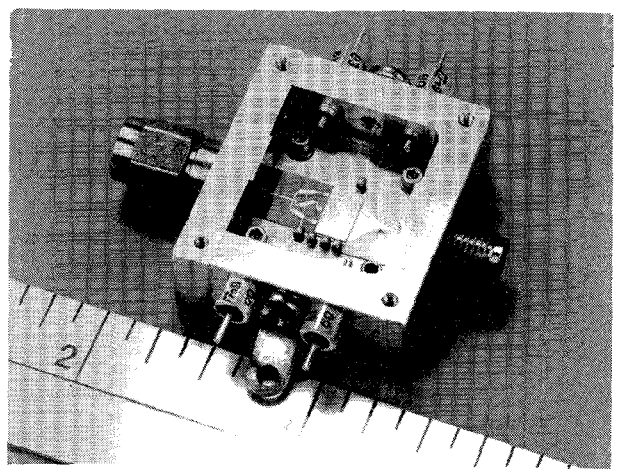

Figure 5. Packaged 4-Watt 20-GHz Amplifier

> 3 watts from 17.8 to 21 GHz (input power = 26 dBm) with 4-watts peak power at 20 GHz. The power-added efficiency averages 25 percent over this band, with 28-percent peak efficiency. Figure 7 shows the performance of a second packaged amplifier processed with 0.25-μm T-gate HFETs. The frequency response has shifted down in frequency so that the > 3-watt output power bandwidth is 16.7 to 20.1 GHz. The power-added efficiency averages 25 percent over this 3.3-GHz band, with 27-percent peak efficiency. These results represent package-level performance with no fixture, connector, or losses of any kind de-embedded.

CONCLUSIONS

0.25-μm HFET technology has demonstrated 4 watts of output power at reasonable efficiency levels at Ka-band. A novel six-way combiner/transformer has been implemented with the partial monolithic circuit.

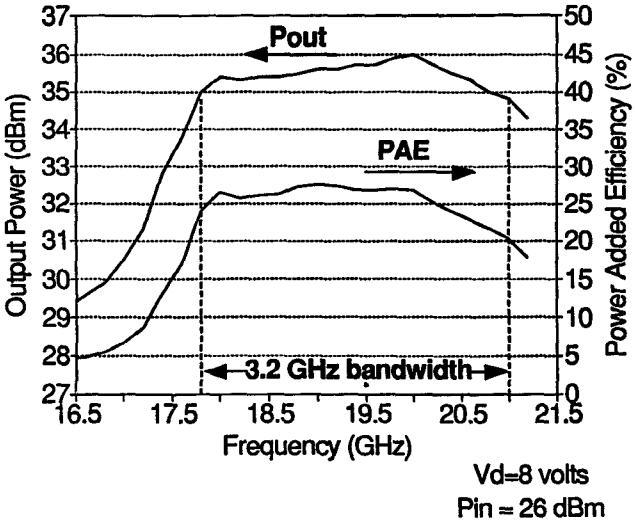

Figure 6. Power and Efficiency for 0.25-μm Delta-Gate HFET Amplifier

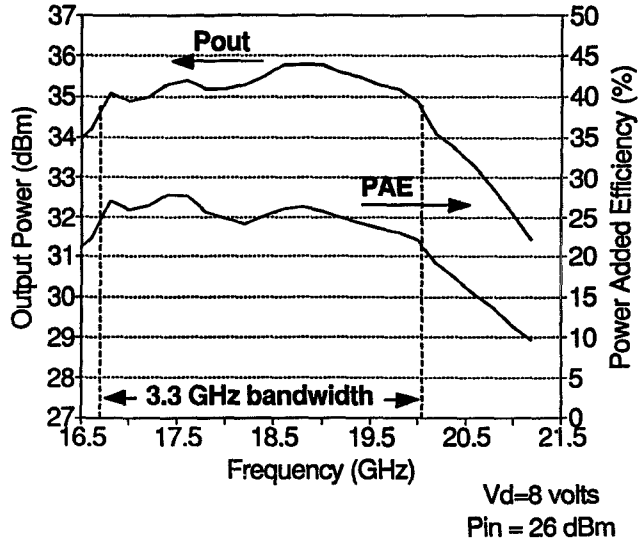

Figure 7. Power and Efficiency for 0.25-μm T-Gate HFET Amplifier

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[1] P. Saunier, W.S. Kopp, H. Q. Tserng, Y. C. Kao, and D. D. Heston, "A Heterostructure FET with 75.8-Percent Power Added Efficiency at 10 GHz," *IEEE MTT-S International Microwave Symposium Digest*, pp. 635-638, 1992.

[2] W. Yau, J. M. Schellenberg, and Y. C. Shih, "A New N-Way Broadband Planar Power Combiner/Divider," *IEEE MTT-S International Microwave Symposium Digest*, pp. 147 - 149, 1986.